

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Chia-Chung Wang et al.  
Assignee: Bridge Semiconductor Corporation  
Title: METHOD OF MAKING A SEMICONDUCTOR CHIP ASSEMBLY WITH A CONDUCTIVE TRACE AND A SUBSTRATE  
Serial No.: Unknown Filed: Herewith  
Examiner: Unknown Group Art Unit: Unknown  
Atty. Docket No.: BDG018

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COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, VA 22313-1450

**INFORMATION DISCLOSURE STATEMENT**

Pursuant to Applicant's duty of disclosure under 37 C.F.R. § 1.56 and §§ 1.97-1.98, Applicant hereby provides the enclosed Form PTO-1449.

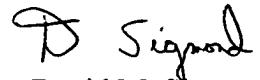
Copies of the documents on the attached Form PTO-1449 are not enclosed because they were previously submitted to or cited by the U.S. Patent Office in U.S. Application Serial No. 09/962,754 filed September 24, 2001, U.S. Application Serial No. 09/878,626 filed June 11, 2001 and/or U.S. Application Serial No. 09/687,619 filed October 13, 2000.

The above-identified application is a continuation-in-part of the '754 application, which is a continuation-in-part of the '626 application, which is a continuation-in-part of the '619 application. Therefore, the documents need not be resubmitted in order to be considered by the Examiner. See M.P.E.P § 609.

The filing of this Information Disclosure Statement shall not be construed as a representation that a search has been made, an admission that any of these documents, alone or in

any combination, is considered to be material to patentability, an admission that any of these documents is prior art as to the above-identified application, or an admission against interest in any manner.

Respectfully submitted,



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Form PTO-1449 U.S. Department of Commerce, Patent and Trademark Office				Atty Docket No. BDG018		Serial No.		
<b>INFORMATION DISCLOSURE STATEMENT</b> (Use several sheets if necessary)				Applicant Chia-Chung Wang et al.				
				Filing Date		Group Art Unit		
<b>U.S. Patent Documents</b>								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA	4,955,523	09/1990	Calomagno et al.	228	179		
	AB	4,970,571	11/1990	Yamakawa et al.	357	71		
	AC	4,984,358	01/1991	Nelson	29	830		
	AD	5,074,947	12/1991	Estes et al.	156	307.3		
	AE	5,106,461	04/1992	Volfson et al.	205	125		
	AF	5,116,463	05/1992	Lin et al.	156	653		
	AG	5,137,845	08/1992	Lochon et al.	437	183		
	AH	5,167,992	12/1992	Lin et al.	427	437		
	AI	5,196,371	03/1993	Kulesza et al.	437	183		
	AJ	5,209,817	05/1993	Ahmad et al.	156	643		
	AK	5,237,130	08/1993	Kulesza et al.	174	260		
	AL	5,260,234	11/1993	Long	437	203		
	AM	5,261,593	11/1993	Casson et al.	228	180.22		
<b>Foreign Patent Documents</b>								
							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AN	EP 0 718 882 A1	06/1996	European Patent Office	H01L	23/057		
	AO	WO 97/38563	10/1997	WIPO	H05K	1/03		
<b>Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)</b>								
	AP	Markstein et al., "Controlling the Variables in Stencil Printing," Electronic Packaging & Production, February 1997, pp. 48-56.						
	AQ	Elenius, "Choosing a Flip Chip Bumping Supplier - Technology an IC Package contractor should look for," Advanced Packaging, March/April 1998, pp. 70-73.						
Examiner		Date Considered						
<p>*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your next communication to Applicant.</p>								

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*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA	5,275,330	01/1994	Issacs et al.	228	180.2		
	AB	5,284,796	02/1994	Nakanishi et al.	437	183		
	AC	5,293,067	03/1994	Thompson et al.	257	668		
	AD	5,327,010	07/1994	Uenaka et al.	257	679		
	AE	5,334,804	08/1994	Love et al.	174	267		
	AF	5,346,750	09/1994	Hatakeyama et al.	428	209		
	AG	5,355,283	10/1994	Marrs et al.	361	760		
	AH	5,358,621	10/1994	Oyama	205	123		
	AI	5,397,921	03/1995	Karnezos	257	779		
	AJ	5,407,864	04/1995	Kim	437	203		
	AK	5,424,245	06/1995	Gurtler et al.	437	183		
	AL	5,438,477	08/1995	Pasch	361	689		
	AM	5,439,162	08/1995	George et al.	228	180.22		
<b>Foreign Patent Documents</b>								
							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AN	WO 99/57762	11/1999	WIPO	H01L	23/48		
	AO							
<b>Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)</b>								
	AP	Erickson, "Wafer Bumping: The Missing Link for DCA," Electronic Packaging & Production, July 1998, pp. 43-46.						
	AQ	Kuchenmeister et al., "Film Chip Interconnection Systems Prepared By Wet Chemical Metallization," IEEE publication 0-7803-4526-6/98, June 1998, 5 pages.						
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*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA	5,447,886	09/1995	Rai	437	183		
	AB	5,454,161	10/1995	Beilin et al.	29	852		
	AC	5,454,928	10/1995	Rogers et al.	205	125		
	AD	5,475,236	12/1995	Yoshizaki	257	48		
	AE	5,477,933	12/1995	Nguyen	174	262		
	AF	5,478,007	12/1995	Marrs	228	180.22		
	AG	5,483,421	01/1996	Gedney et al.	361	771		
	AH	5,484,647	01/1996	Nakatani et al.	428	209		
	AI	5,487,218	01/1996	Bhatt et al.	29	852		
	AJ	5,489,804	02/1996	Pasch	257	778		
	AK	5,493,096	02/1996	Koh	219	121.71		
	AL	5,508,229	04/1996	Baker	437	183		
	AM	5,525,065	06/1996	Sobhani	439	67		
<b>Foreign Patent Documents</b>							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AN							
	AO							
<b>Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)</b>								
	AP	Ghaffarian, "Long Time BGA Assembly Reliability," Advancing Microelectronics, Vol. 25, No. 6, September/October 1998, pp. 20-23.						
	AQ	U.S. Application Serial No. 09/465,024, filed December 16, 1999, entitled "Bumpless Flip Chip Assembly With Solder Via"						
Examiner			Date Considered					
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<b>U.S. Patent Documents</b>								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA	5,536,973	07/1996	Yamaji	257	737		
	AB	5,542,601	08/1996	Fallon et al.	228	119		
	AC	5,547,740	08/1996	Higdon et al.	428	209		
	AD	5,556,810	09/1996	Fujitsu	437	209		
	AE	5,556,814	09/1996	Inoue et al.	437	230		
	AF	5,564,181	10/1996	Dineen et al.	29	841		
	AG	5,572,069	11/1996	Schneider	257	690		
	AH	5,576,052	11/1996	Arledge et al.	427	98		
	AI	5,583,073	12/1996	Lin et al.	439	183		
	AJ	5,595,943	01/1997	Itabashi et al.	437	230		
	AK	5,599,744	02/1997	Koh et al.	437	195		
	AL	5,611,140	03/1997	Kulesza et al.	29	832		
	AM	5,611,884	03/1997	Bearinger et al.	156	325		
<b>Foreign Patent Documents</b>								
							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AN							
	AO							
<b>Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)</b>								
	AP	U.S. Application Serial No. 09/464,562, filed December 16, 1999, entitled "Bumpless Flip Chip Assembly With Strips And Via-Fill"						
	AQ	U.S. Application Serial No. 09/464,561, filed December 16, 1999, entitled "Bumpless Flip Chip Assembly With Strips-In-Via And Plating"						
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*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	5,613,296	03/1997	Kurino et al.	29	852	
	AB	5,614,114	03/1997	Owen	219	121.66	
	AC	5,615,477	04/1997	Sweitzer	29	840	
	AD	5,619,791	04/1997	Lambrecht Jr. et al.	29	852	
	AE	5,627,405	05/1997	Chillara	257	668	
	AF	5,627,406	05/1997	Pace	257	700	
	AG	5,633,204	05/1997	Tago et al.	438	614	
	AH	5,637,920	06/1997	Loo	257	700	
	AI	5,641,113	06/1997	Somaki et al.	228	180.22	
	AJ	5,645,628	07/1997	Endo et al.	106	1.23	
	AK	5,646,067	07/1997	Gaul	437	180	
	AL	5,648,686	07/1997	Hirano et al.	257	778	
	AM	5,654,584	08/1997	Fujitsu	257	666	

**Foreign Patent Documents**

							Translation
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**Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)**

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Examiner	Date Considered
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*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA	5,656,858	08/1997	Kondo et al.	257	737		
	AB	5,663,598	09/1997	Lake et al.	257	737		
	AC	5,665,652	09/1997	Shimizu	438	127		
	AD	5,666,008	09/1997	Tomita et al.	257	778		
	AE	5,669,545	09/1997	Pham et al.	228	1.1		
	AF	5,674,785	10/1997	Akram et al.	437	217		
	AG	5,674,787	10/1997	Zhao et al.	437	230		
	AH	5,682,061	10/1997	Khandros et al.	257	666		
	AI	5,691,041	11/1997	Frankeny et al.	428	209		
	AJ	5,722,162	03/1998	Chou et al.	29	852		
	AK	5,723,369	03/1998	Barber	438	106		
	AL	5,731,223	03/1998	Padmanabhan	437	183		
	AM	5,736,456	04/1998	Akram	438	614		
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*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA	5,739,585	04/1998	Akram et al.	257	698		
	AB	5,744,859	04/1998	Ouchida	257	668		
	AC	5,757,071	05/1998	Bhansali	257	697		
	AD	5,757,081	05/1998	Chang et al.	257	778		
	AE	5,764,486	06/1998	Pendse	361	774		
	AF	5,774,340	06/1998	Chang et al.	361	771		
	AG	5,789,271	08/1998	Akram	438	18		
	AH	5,798,285	08/1998	Bentlage et al.	438	108		
	AI	5,801,072	09/1998	Barber	438	107		
	AJ	5,801,447	09/1998	Hirano et al.	257	778		
	AK	5,803,340	09/1998	Yeh et al.	228	56.3		
	AL	5,804,771	09/1998	McMahon et al.	174	255		
	AM	5,808,360	09/1998	Akram	257	738		
<b>Foreign Patent Documents</b>								
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*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA	5,811,879	09/1998	Akram	257	723		
	AB	5,817,541	10/1998	Averkiou et al.	438	107		
	AC	5,822,856	10/1998	Bhatt et al.	29	832		
	AD	5,834,844	11/1998	Akagawa et al.	257	734		
	AE	5,861,666	01/1999	Bellaar	257	686		
	AF	5,863,816	01/1999	Cho	438	123		
	AG	5,870,289	02/1999	Tokuda et al.	361	779		
	AH	5,883,435	03/1999	Geffken et al.	257	758		
	AI	5,925,931	07/1999	Yamamoto	257	737		
	AJ	5,994,222	11/1999	Smith et al.	438	689		
	AK	6,012,224	01/2000	DiStefano et al.	29	840		
	AL	6,013,877	01/2000	Degani et al.	174	264		
	AM	6,018,196	01/2000	Noddin	257	777		
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*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA	6,020,561	02/2000	Ishida et al.	174	261		
	AB	6,037,665	03/2000	Miyazaki	257	773		
	AC	6,046,909	04/2000	Joy	361	748		
	AD	6,084,297	06/2000	Brooks et al.	257	698		
	AE	6,084,781	07/2000	Klein	361	771		
	AF	6,103,552	08/2000	Lin	438	113		
	AG	6,103,992	08/2000	Noddin	219	121.71		
	AH	6,127,204	10/2000	Isaacs et al.	438	106		
	AI							
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	AK							
	AL							
	AM							
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	AA	4,442,967	04/1984	van de Pas et al.	228	159		
	AB	4,661,192	04/1987	McShane	156	292		
	AC	4,717,066	01/1988	Goldenberg et al.	228	179		
	AD	4,750,666	06/1988	Neugebauer et al.	228	160		
	AE	4,807,021	02/1989	Okumura	357	75		
	AF	4,925,083	05/1990	Farassat et al.	228	102		
	AG	4,937,653	06/1990	Blonder et al.	357	68		
	AH	5,014,111	05/1991	Tsuda et al.	357	68		
	AI	5,060,843	10/1991	Yasuzato et al.	228	179		
	AJ	5,090,119	02/1992	Tsuda et al.	29	843		
	AK	5,172,851	12/1992	Matsushita et al.	228	179		
	AL	5,294,038	03/1994	Nakano et al.	228	179.1		
	AM	5,364,004	11/1994	Davidson	228	1.1		
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	AA	5,485,949	01/1996	Tomura et al.	228	180.5		
	AB	5,686,353	11/1997	Yagi et al.	437	183		
	AC	5,813,115	09/1998	Misawa et al.	29	832		
	AD	6,017,812	01/2000	Yonezawa et al.	438	613		
	AE	6,088,236	07/2000	Tomura et al.	361	783		
	AF	6,159,770	12/2000	Tetaka et al.	438	112		
	AG							
	AH							
	AI							
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	AB	Document	Date	Country	Class	Subclass	Yes	No
<b>Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)</b>								
	AC	U.S. Application Serial No. 09/120,408, filed July 22, 1998, entitled "Flip Chip Assembly With Via Interconnection"						
	AD	U.S. Application Serial No. 09/643,212, filed August 22, 2000, entitled "Semiconductor Chip Assembly With Simultaneously Electroplated Contact Terminal and Connection Joint"						
	AE	U.S. Application Serial No. 09/643,214, filed August 22, 2000, entitled "Semiconductor Chip Assembly with Simultaneously Electrolessly Plated Contact Terminal and Connection Joint"						
	AF	U.S. Application Serial No. 09/643,213, filed August 22, 2000, entitled "Method Of Making A Support Circuit For A Semiconductor Chip Assembly"						
	AG	U.S. Application Serial No. 09/643,445, filed August 22, 2000, entitled "Method Of Making A Semiconductor Chip Assembly"						
	AH	U.S. Application Serial No. 09/665,928, filed September 20, 2000, entitled "Semiconductor Chip Assembly With Ball Bond Connection Joint"						
	AI	U.S. Application Serial No. 09/665,931, filed September 20, 2000, entitled "Method Of Making A Support Circuit With A Tapered Through-Hole For A Semiconductor Chip Assembly"						
	AJ	U.S. Application Serial No. 09/677,207, filed October 2, 2000, entitled "Method Of Making A Semiconductor Chip Assembly With A Conductive Trace Subtractively Formed Before And After Chip Attachment"						
Examiner		Date Considered						
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					Filing Date		Group Art Unit	
<b>U.S. Patent Documents</b>								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA							
<b>Foreign Patent Documents</b>								
							Translation	
	AB						Yes	No
<b>Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)</b>								
	AC	U.S. Application Serial No. 09/865,367, filed May 24, 2001, entitled "Semiconductor Chip Assembly With Simultaneously Electroplated Contact Terminal and Connection Joint"						
	AD	U.S. Application Serial No. 09/864,555, filed May 24, 2001, entitled "Semiconductor Chip Assembly with Simultaneously Electrolessly Plated Contact Terminal and Connection Joint"						
	AE	U.S. Application Serial No. 09/864,773, filed May 24, 2001, entitled "Semiconductor Chip Assembly With Ball Bond Connection Joint"						
Examiner			Date Considered					
<p><b>*EXAMINER:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your next communication to Applicant.</p>								